Simple Circuit Extensions for XOR in PTIME

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Outline

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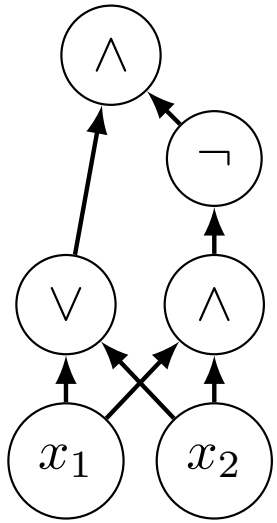

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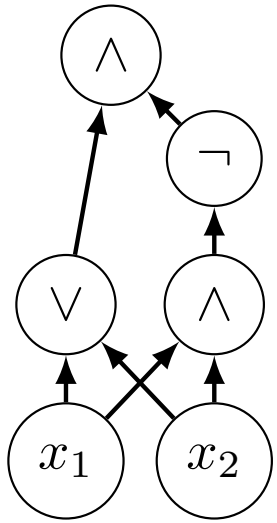

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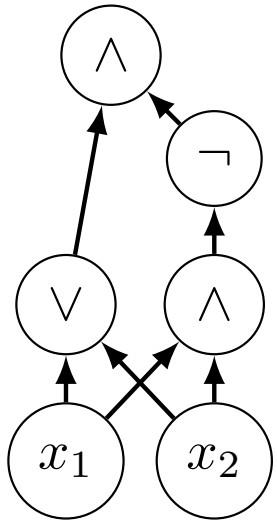
- $CC(f)$:= size of the smallest circuit computing f



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  - DNF-MCSP [Masek 1979]
  - OR-AND-MOD-MCSP [Hirahara, Oliveira, Santhanam 2018]
  - Multi-output MCSP [Ilango, Loff, Oliviera 2020]

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  - Barriers to proving MCSP without added assumptions

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- Can we use XOR?

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Corollary (Main Corollary)

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- Analyzing *structure* will help us apply/bypass our algorithm

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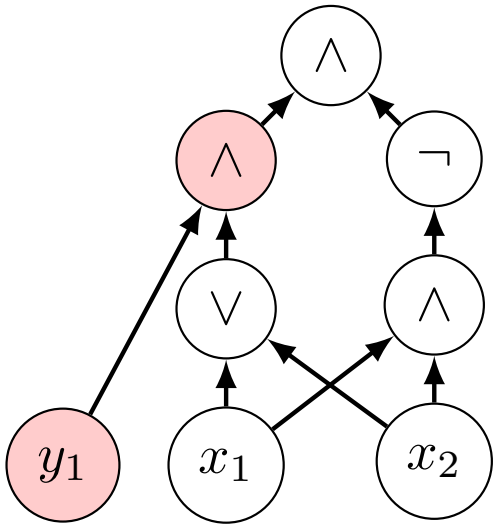

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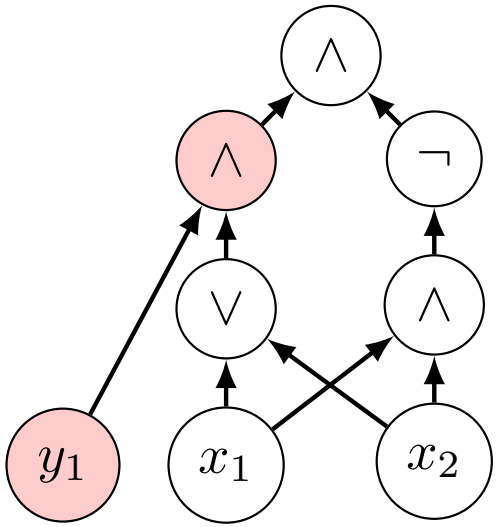

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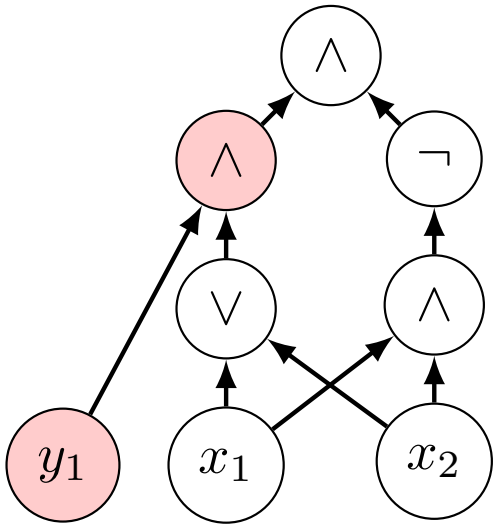

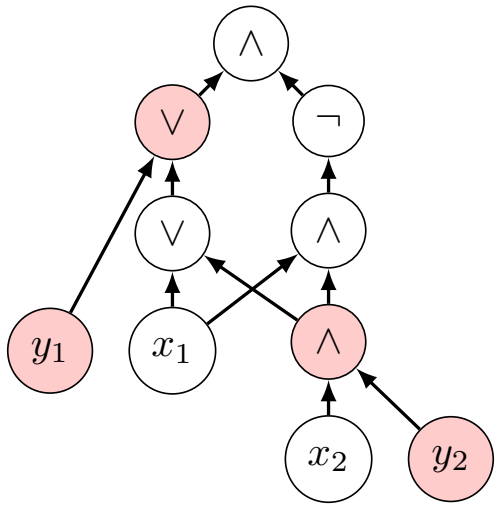

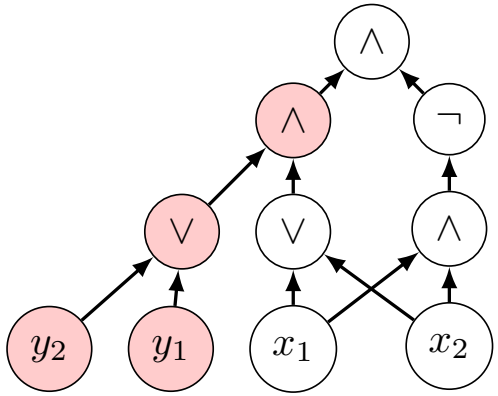

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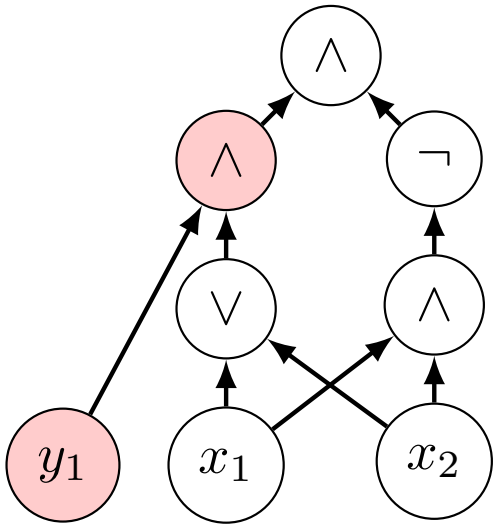

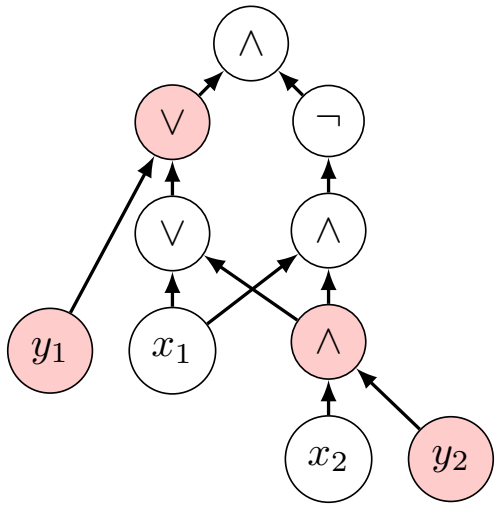

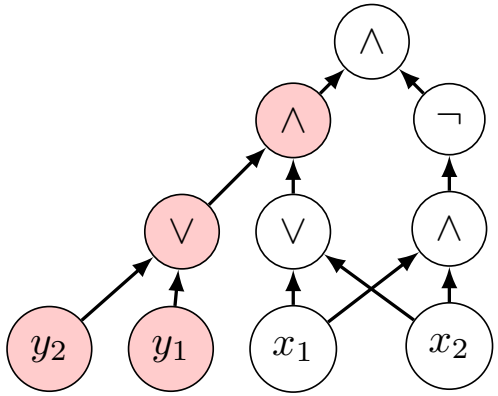

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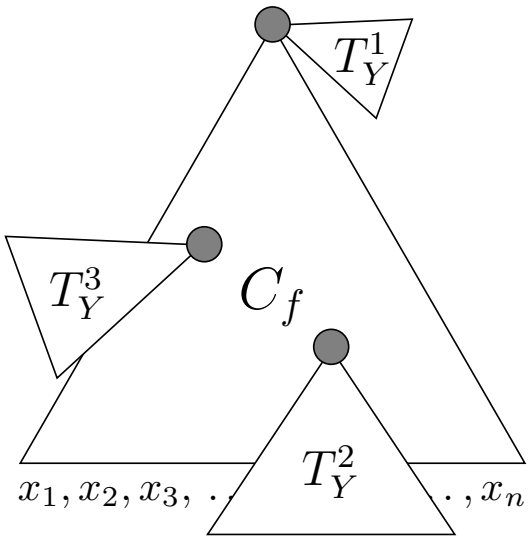

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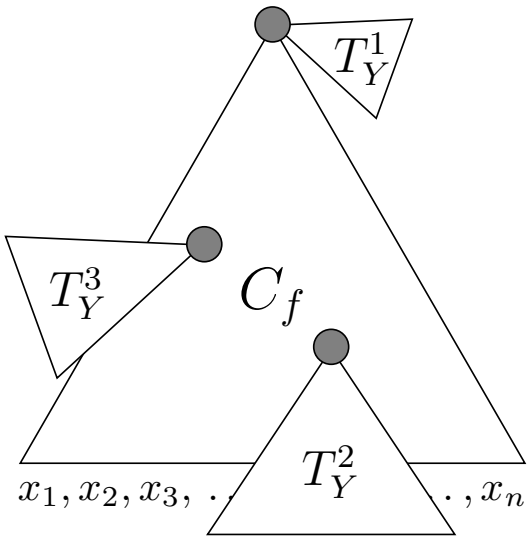

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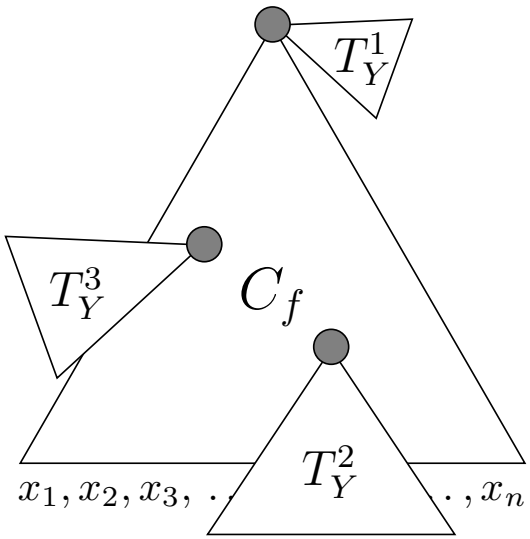
- If these are limited, then we could try to brute force over all possible ways to add the subformulas



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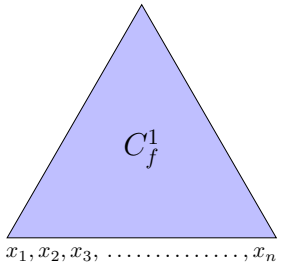

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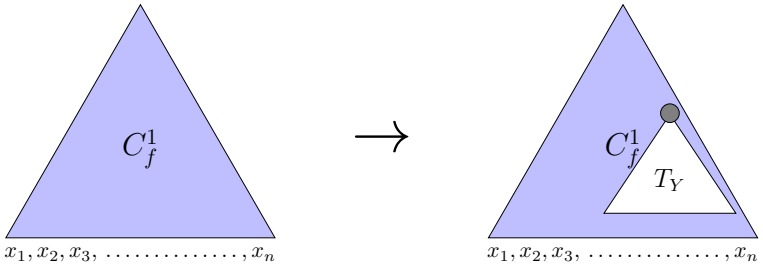

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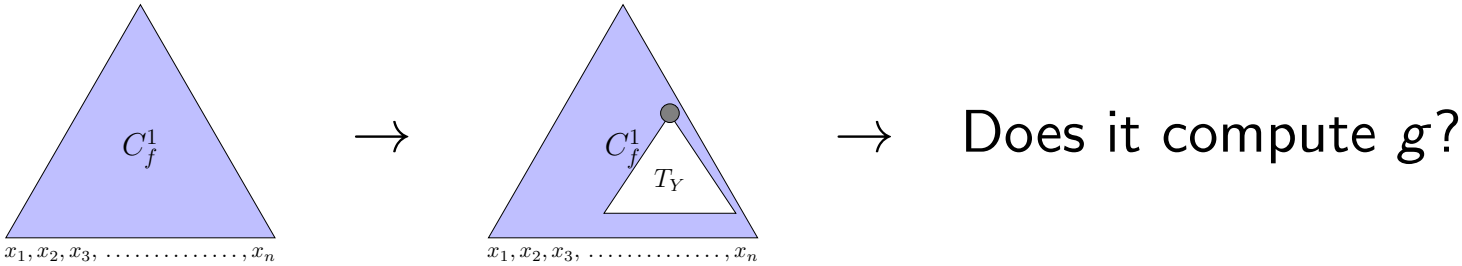

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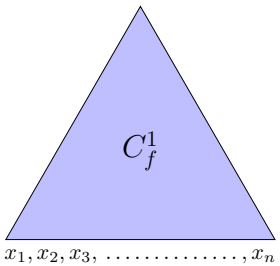

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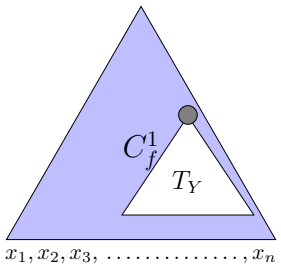

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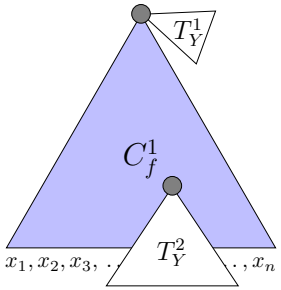

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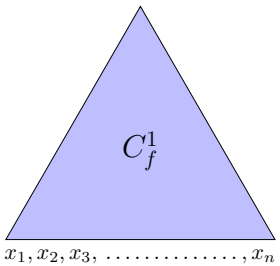

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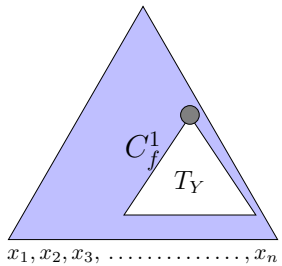

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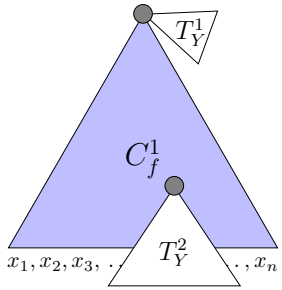

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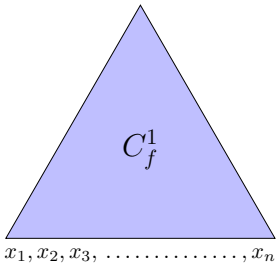

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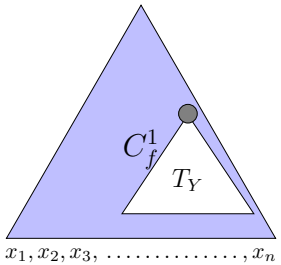

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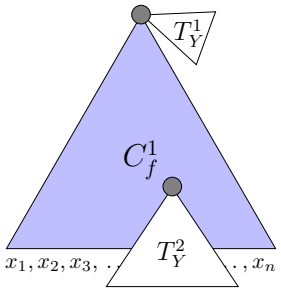

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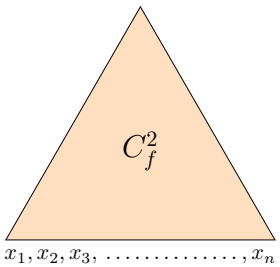

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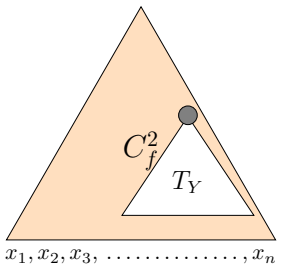

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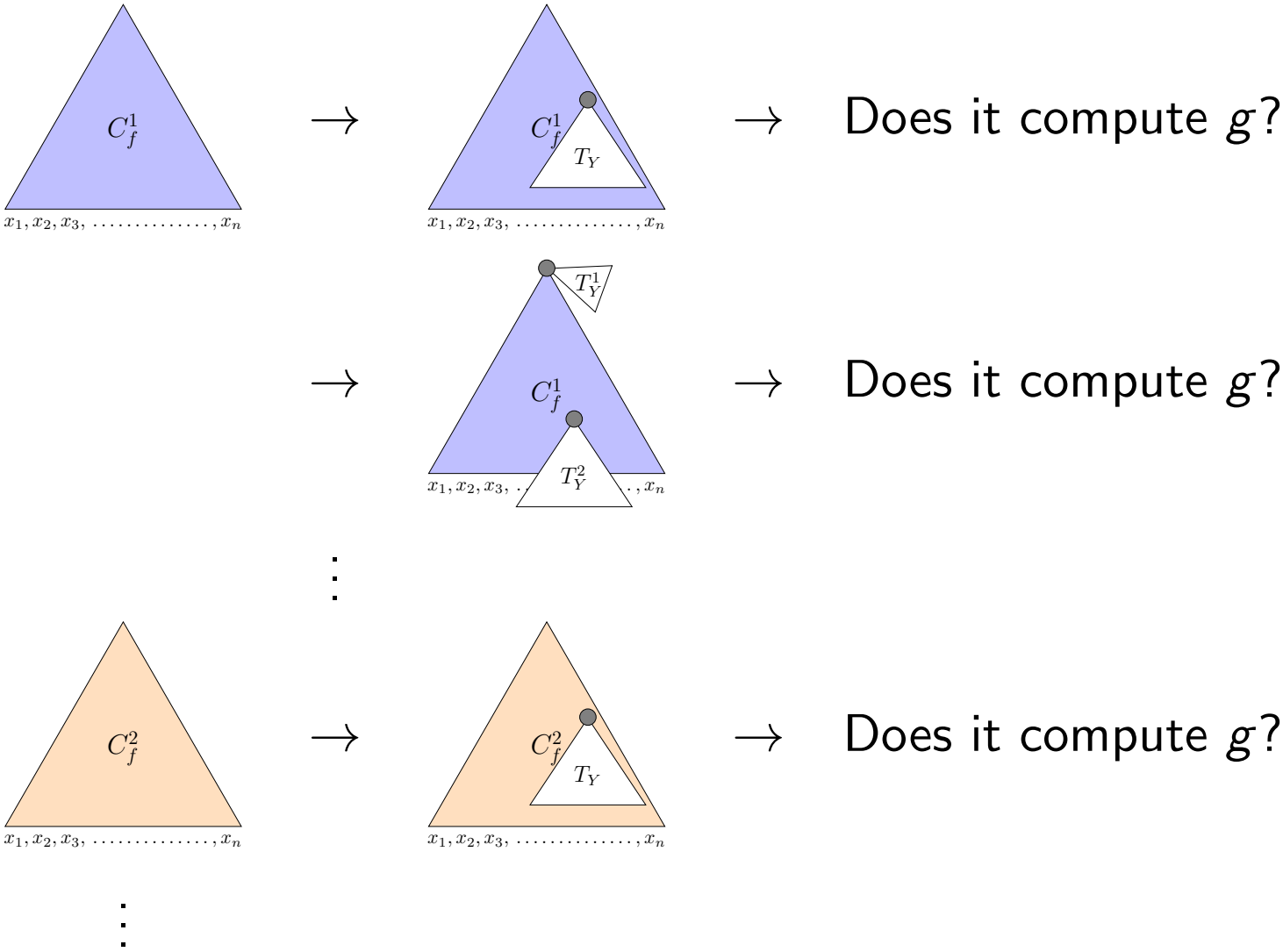

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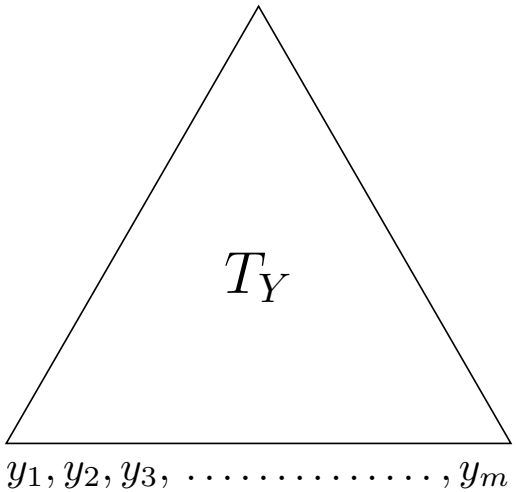

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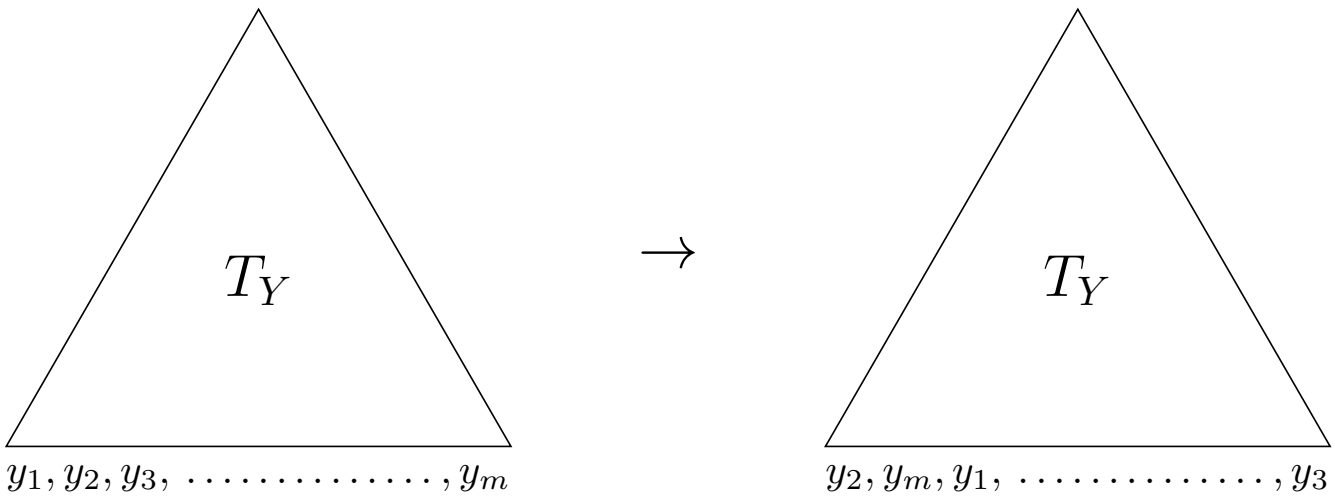

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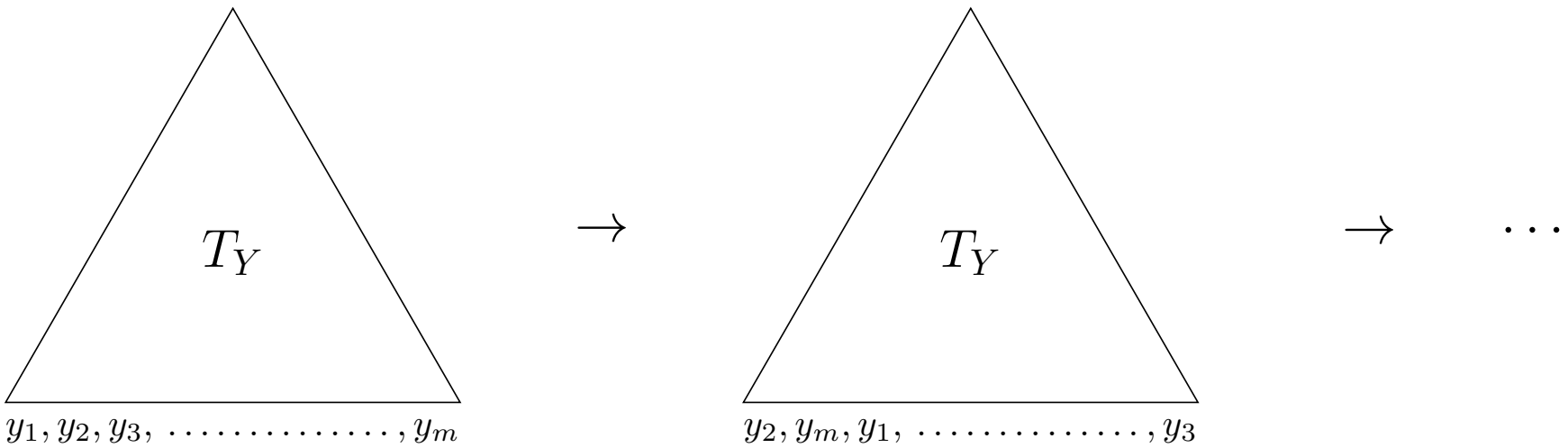

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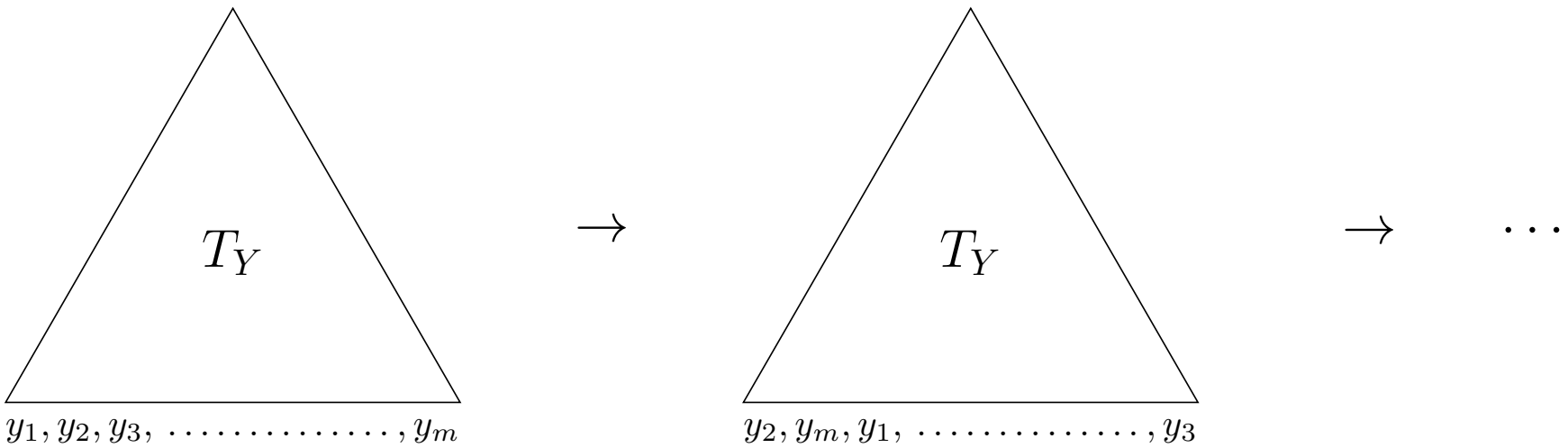

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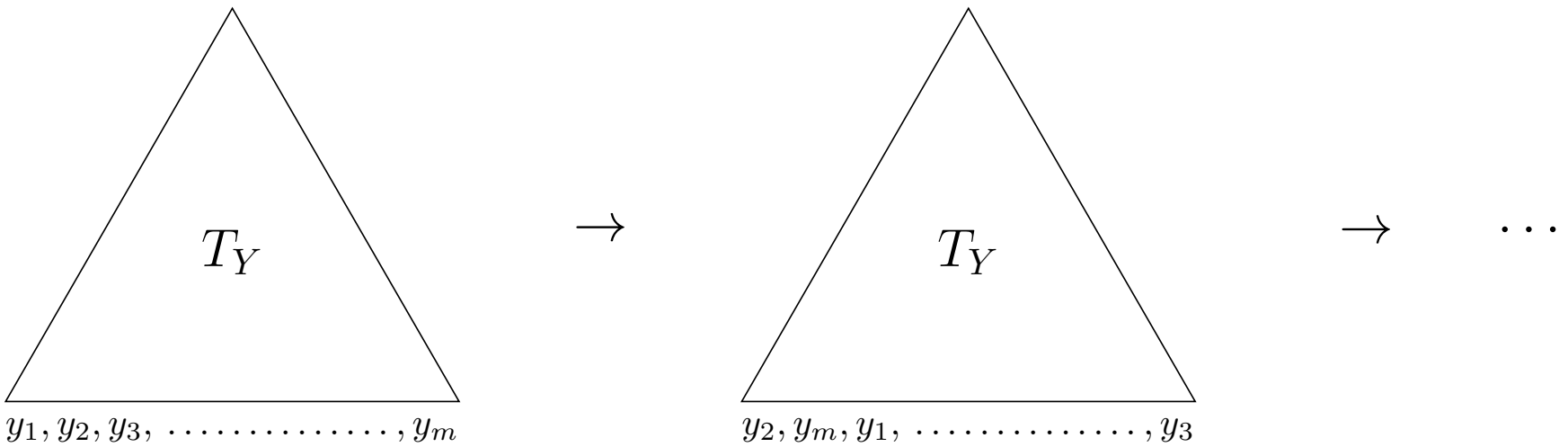

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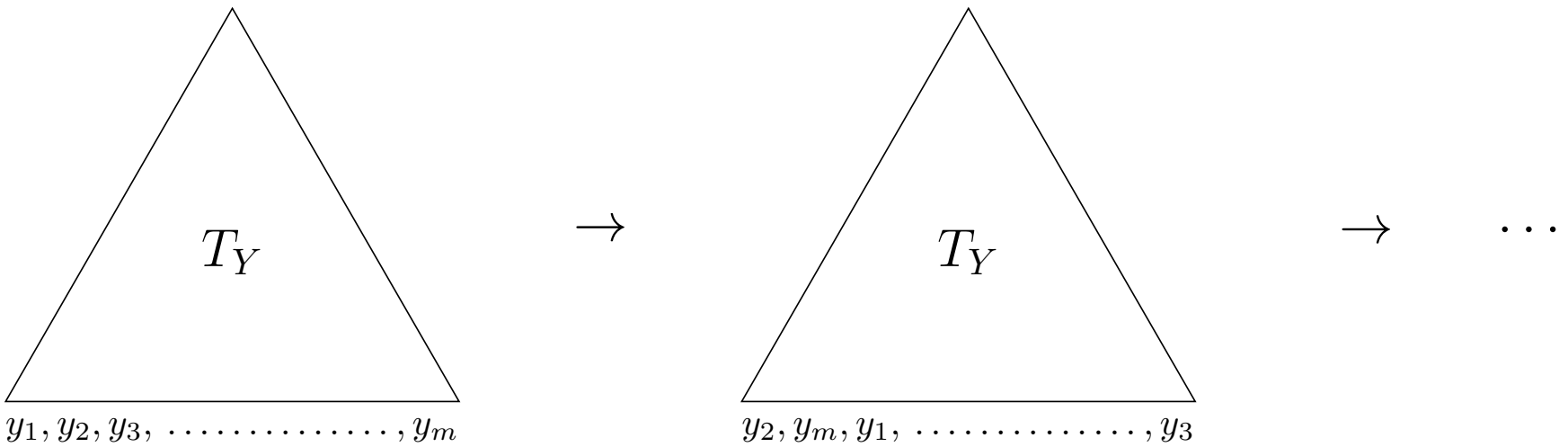

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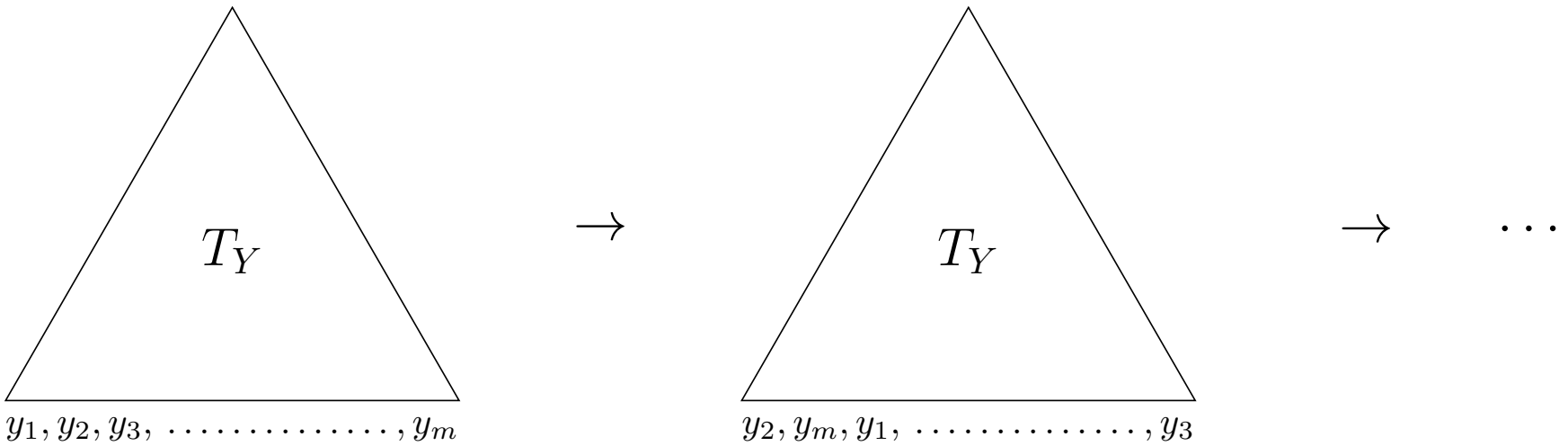

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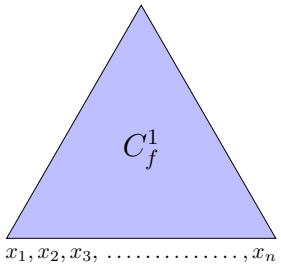

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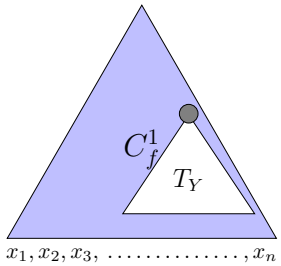

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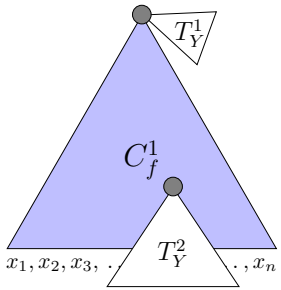

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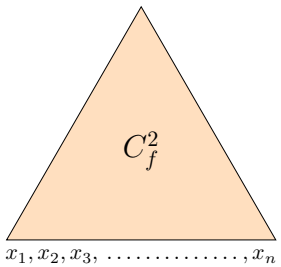

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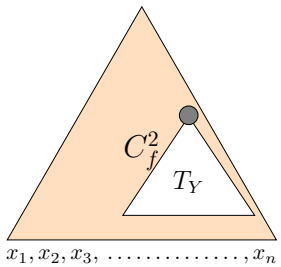

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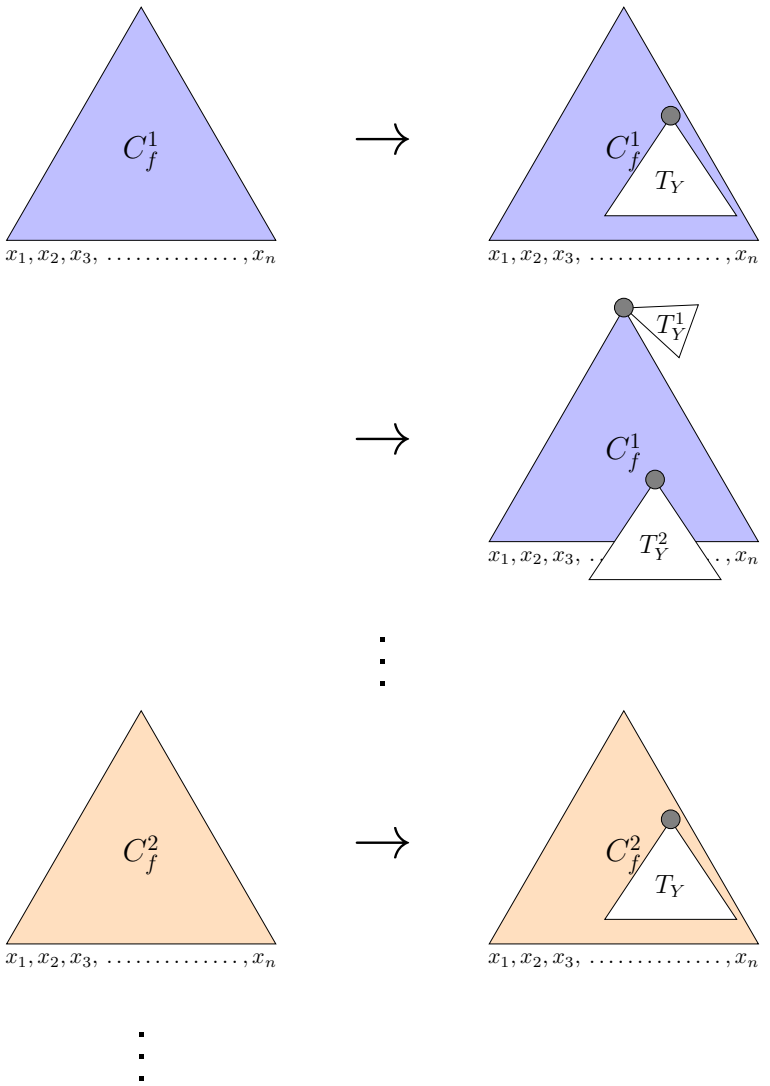

Inner Loops Feasible By:

- Y-Tree Decomposition
- Truth-Table Isomorphism
- $|C_f|$ is linear
- Low Fan-Out

→ Is it tt-isomorphic to g?

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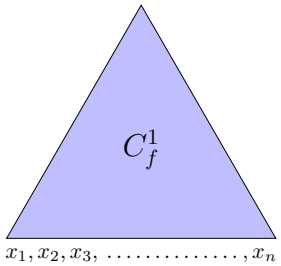

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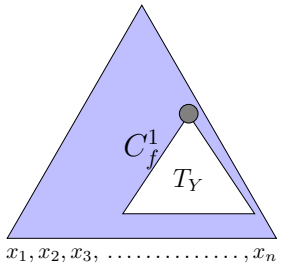

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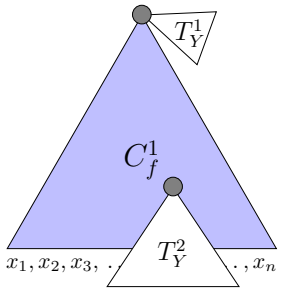

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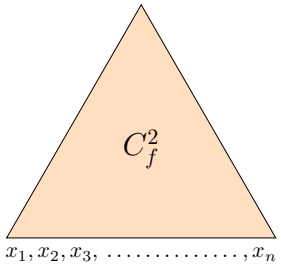

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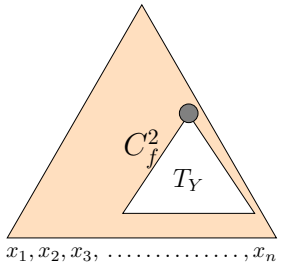

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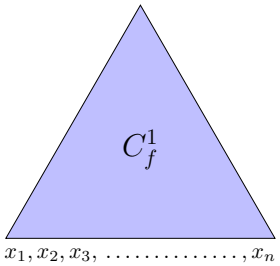

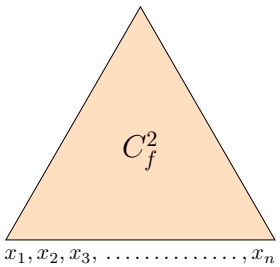

Outer Loop Feasible By:

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Characterizing XOR

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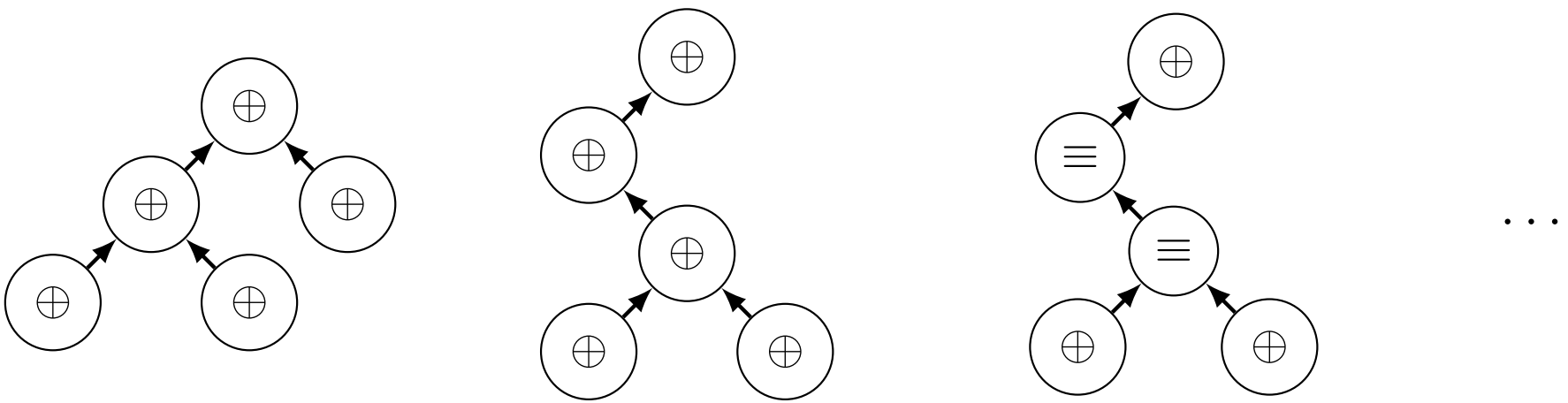

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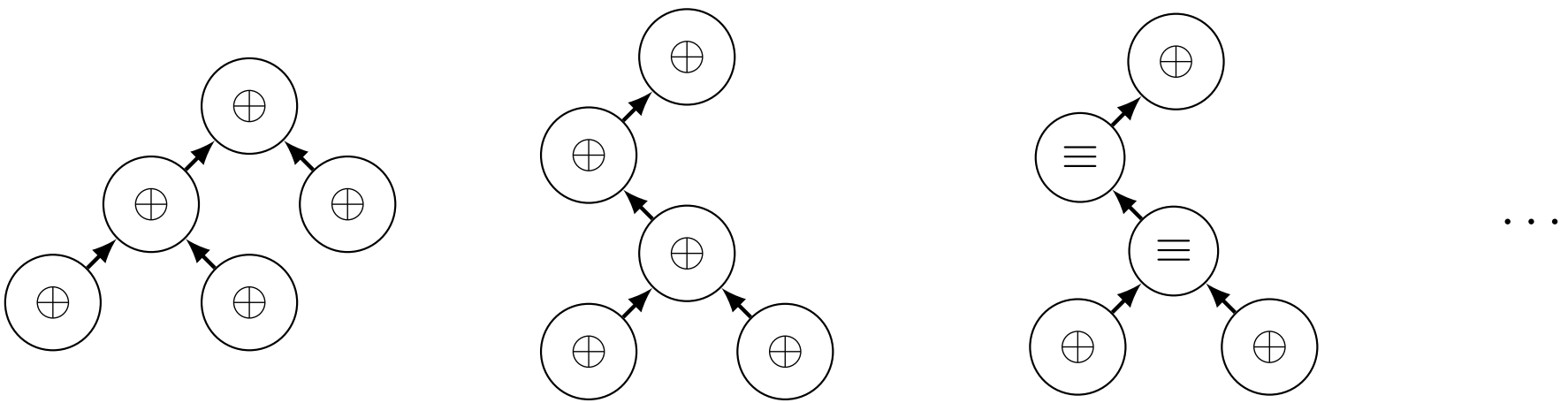

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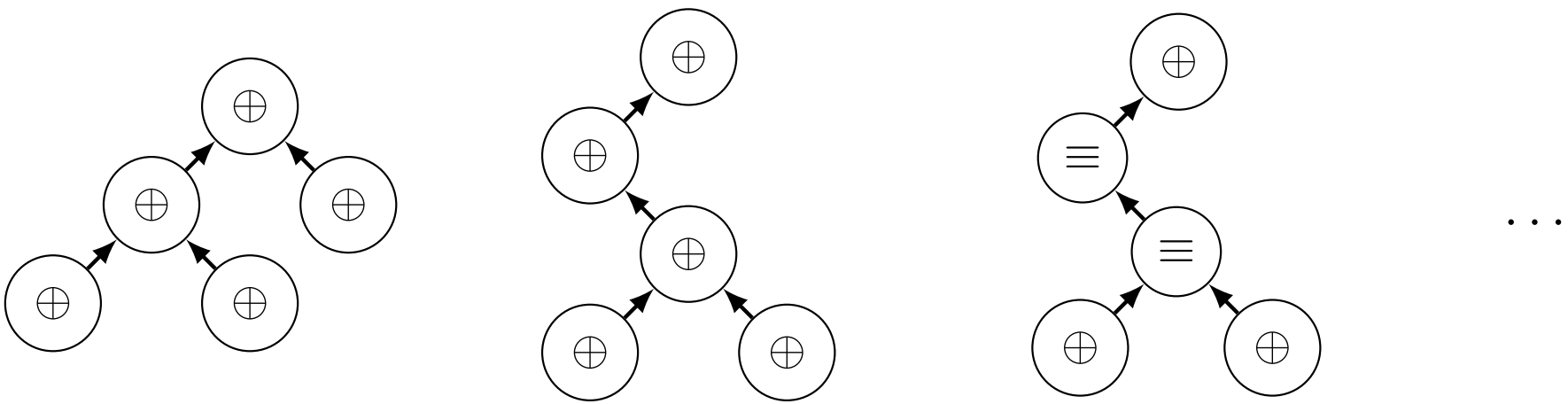

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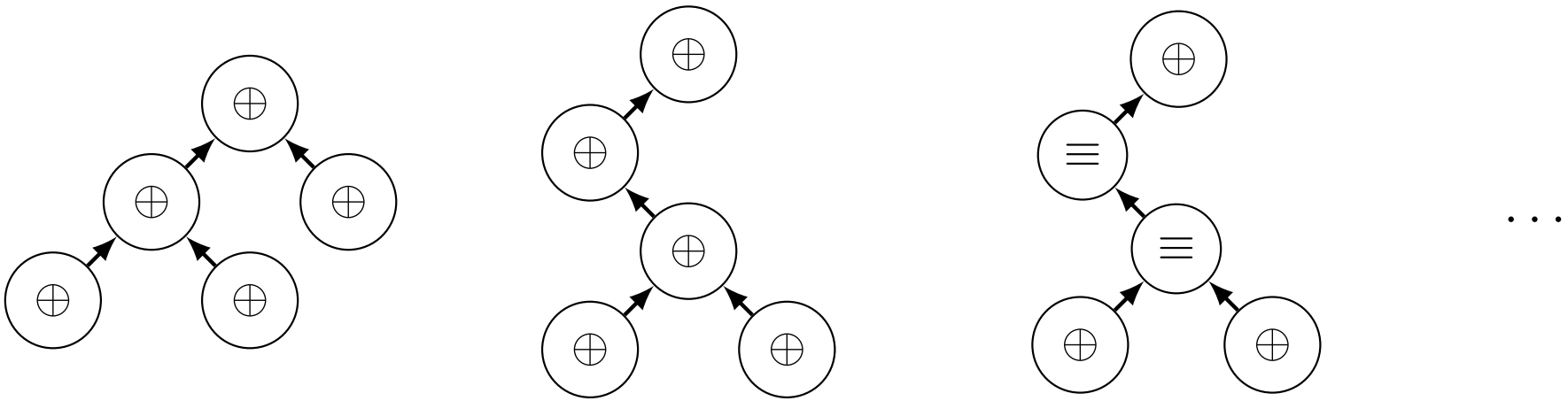
- This structure + our FPT algorithm gives us that XOR-SEP is in P



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Sum Mod 2^k	$4n - O(1)$	$7n - o(n)$	NO?
Multiplexer	$2(n-1)$	$2n + O(\sqrt{n})$	YES?
Well-Mixed	$5n - o(n)$	poly	MAYBE?
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- More generally, can we learn more about the *structure* of optimal circuits, not just bounds?

Thank You!

https://cs-people.bu.edu/ndang

Ngu (Nathan) Dang

Boston University

Email: ndang@bu.edu

Building an XOR_2 Widget

- Let C be an optimal circuit for XOR_n

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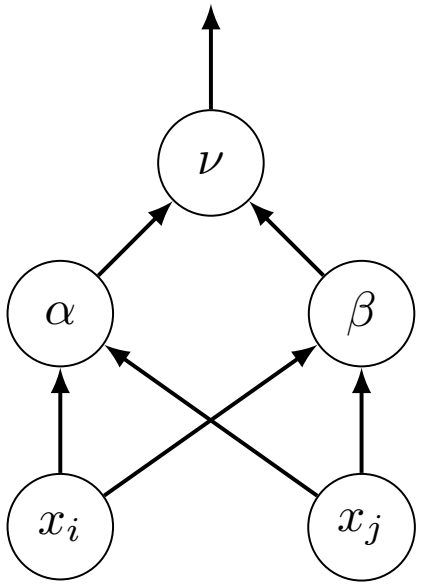

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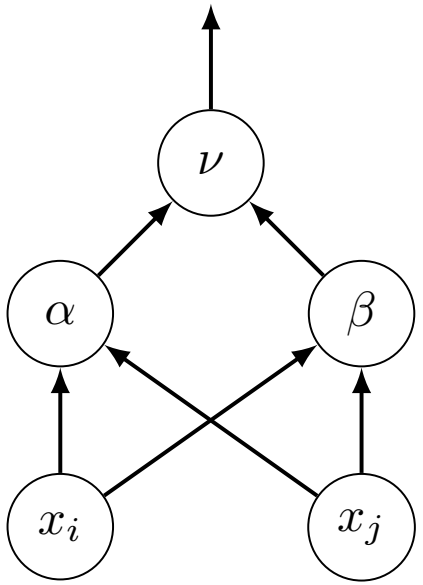

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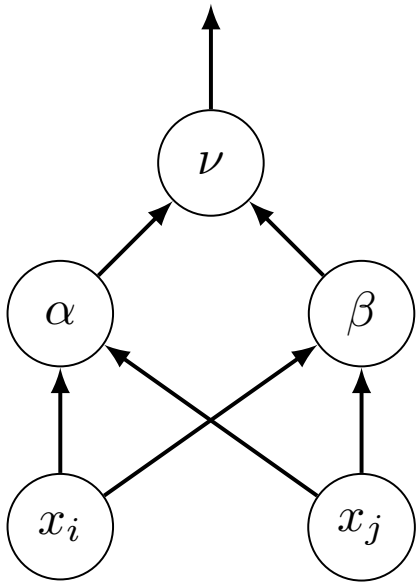

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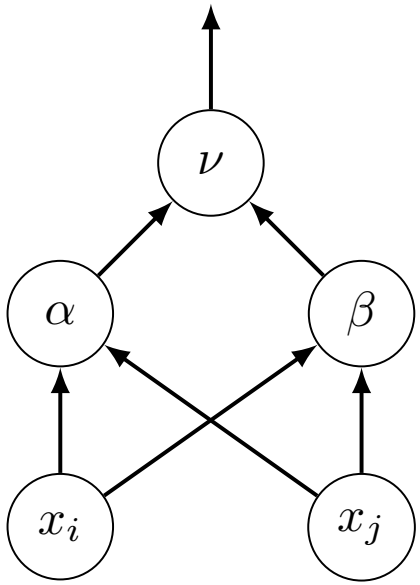
  - Substitute $x_i \leftarrow b$ and simplify



Building an XOR_2 Widget

- Let C be an optimal circuit for XOR_n
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- Goal: Build up $(\neg)\mathrm{XOR}_2$ widget around α
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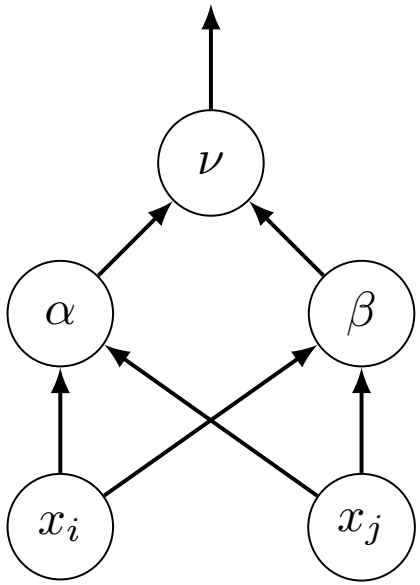
  - Violate some fact about $\mathrm{XOR}_n\restriction_{x_i \leftarrow b}$



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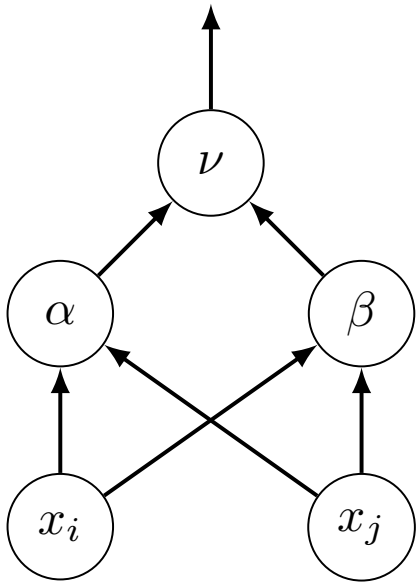

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    - Like x_j is no longer read by the circuit
    - Or we eliminate too many gates